Independent Claim 6, as amended, requires and positively recites, "a first processor for performing scalar processing, said first processor comprising a core, **a program memory and a local memory**", "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "a memory circuit **for coupling said local memory of said first processor to said local memory of said second processor**".

RECEIVED
JUL 18 2000
TC 2700 MAIL ROOM

The Examiner states that Aoyama teaches the claimed invention, comprising: a first processor for performing scalar processing (e.g., fig. 1, el. 600), comprising a core, a local memory, and a program memory (e.g., fig. 1, els. 601 and 602; and col. 5, lines 47 et seq.); a second processor for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core, a local memory and a program memory (e.g., fig. 1, els. 501 and 502; and col. 8, lines 4 et seq.); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, col. 5-6); and a memory circuit for coupling the local memory of the first processor to local memory of the second processor (e.g., fig. 1, el. 800)(Office Action dated 1/19/00, page 5, line 17 page 6, line 6). Applicants respectfully traverse.

The Aoyama reference discloses a device in which the vector processor comprises a vector register 502 coupling vector arithmetic 501 to address translation 503. Address translation 503 is coupled to main storage 700 (which is external to vector processor (VP)). Accordingly, since main storage 700 is not part of vector processor (VP), it is not an "on-board" local memory or program memory that is part of vector process (VP). The Examiner relies upon col. 8, lines 4 et seq. to support her argument that Aoyama's vector processor contains both a **program memory and a local memory**. The Examiner is obviously relying upon main storage (MS) 1 as being one of the program memory or local memory - e.g., the teaching that "an address generated by the vector instruction address generate circuit 200 is sent to the main storage 1, and a vector instruction read from the main storage 1 is sent to a register 201" (col. 8, lines 12-15). Unfortunately, the Examiner's reliance on Aoyama is misplaced. Aoyama discloses that "the address generate circuit 200 is configured in the same fashion as the scalar instruction read circuit of FIG. 4 (col. 8, lines 9-

12). Aoyama further discloses that MS 1 corresponds to main storage 700 in FIG. 1 (col. 5, lines 31-32). Main storage 700 is NOT part of vector processor 500 or scalar processor 600. Accordingly, Aoyama fails to teach or suggest, "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", as is required by Claim 6. Moreover, vector processor (VP) has no equivalent to buffer storage 602 of scalar processor 600, which the Examiner relies upon as one of the memories for scalar processor 600. The 35 U.S.C. 102(e) rejection of Claim 6 is overcome.

Moreover, there is no teaching or suggestion in the art that would have motivated one of ordinary skill in the art at the time of the invention to re-engineer the Aoyama device to include an internal memory, as is required by Claim 6, without the improper hindsight provided by Applicants' disclosure. As a result, Claim 6 stands allowable.

Claims 7-15, 17, 19, 34 and 35 stand allowable as depending from allowable claims and include further limitation not taught or suggested by the references of record.

Claim 7 further defines the apparatus of Claim 6, wherein said second processor is the main processor of said apparatus. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. Moreover, assuming, arguendo, that Ngai et al discloses "the use of a main processor", it fails to overcome the previously identified deficiency of the Aoyama reference.

Claim 8 further defines the apparatus of Claim 7, wherein said first processor is a microprocessor. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 7.

Claim 9 further defines the apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP". The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 7.

Claim 10 further defines the apparatus of Claim 6, wherein said program memory of said first processor is ROM memory. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 11 further defines the apparatus of Claim 6, wherein said local memory of said first processor is RAM memory. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 12 further defines the apparatus of Claim 6, wherein said program memory of said second processor is ROM memory. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 13 further defines the apparatus of Claim 6, wherein said local memory of said second processor is RAM memory. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 14 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 15 further defines the apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 17 further defines the apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. The

Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 19 further defines the apparatus of Claim 6, wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions: integers corresponding to arithmetic and logic operations on integer numbers; transfer corresponding to the transfer operations between a register in said protocol processor and memory; and monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

Claim 34 further defines the apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. In addition to the previously identified deficiency of Aoyama as applied to Claim 6, Applicants traverse the Examiner's stated Official Notice that "both the concept and advantages of providing integer instructions corresponding to ALU operations on integer numbers; providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and task which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type are well known and expected in the art - it would have been obvious to one or ordinary skill in the art to include a protocol processor; and DSP and array processor into Aoyama because it would allow scalar processing to encompass high level teaks; and signal processing and matrix computations to be performed (Office Action dated 01/19/00, page 10, lines 3-11).

Applicants further respectfully submit that the "level of skill in the art" is the level "at the time of the invention - June 1991", not the present level of skill in the art. The Examiner has provided no pre-June 1991 motivation in the art for such a modification.

Claim 35 further defines the apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and a matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type. The Aoyama reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6. In addition to the previously identified deficiency of Aoyama as applied to Claim 6, Applicants traverse the Examiner's stated Official Notice that "both the concept and advantages of providing integer instructions corresponding to ALU operations on integer numbers; providing scalar processing encompassed a high level task which is the monitoring of an application or the management of functioning and task which are generally carry out by hard-wired logic which are the protocol processing; and vector processing including signal processing tasks generally carrying out by a DSP and the use of array processor type are well known and expected in the art - it would have been obvious to one or ordinary skill in the art to include a protocol processor; and DSP and array processor into Aoyama because it would allow scalar processing to encompass high level teaks; and signal processing and matrix computations to be performed (Office Action dated 01/19/00, page 10, lines 3-11).

Applicants further respectfully submit that the "level of skill in the art" is the level "at the time of the invention - June 1991", not the present level of skill in the art. The Examiner has provided no pre-June 1991 motivation in the art for such a modification.

Independent Claim 36 requires and positively recites, "a first processor comprising a core, **a program memory and a local memory**", "a second processor comprising a core, **a program memory and a local memory**", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said first processor to said local memory of said second processor**".

Independent Claim 37 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core**, a program memory and a local memory**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

Independent Claim 38 requires and positively recites, "a **main processor** comprising a core, a program memory and a local memory", "a **protocol processor** comprising a core, a program memory and a local memory, **said protocol processor being suited to execute tasks to which the main processor is not suited**", "a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor" and "a common memory coupling said local memory of said main processor to said local memory of said protocol processor".

Independent Claim 39 requires and positively recites, "a main processor comprising a core, **a program memory and a local memory**", "a protocol processor comprising a core, **a program memory and a local memory**, said protocol processor being suited to execute tasks to which the main processor is not suited", "a synchronizing circuit for coupling said core of said first processor to said core of said second processor" and "**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**".

The Examiner states that Aoyama teaches the claimed invention, comprising: a first processor for performing scalar processing (e.g., fig. 1, el. 600), comprising a core, a local memory, and a program memory (e.g., fig. 1, els. 601 and 602; and col. 5, lines 47 et seq.), wherein the first processor being suited to execute tasks to which the main processor is not suited; a second processor for performing vector processing (e.g., fig. 1, el. 500, vector processor), comprising a core, a local memory and a program memory (e.g., fig. 1, els. 501 and 502; and col. 8, lines 4 et seq.); a synchronizing circuit for coupling the core of the first processor to the core of the second processor (e.g., fig. 1, els 810 or 800a, col. 5-6); and one and only one memory circuit for coupling

the local memory of the first processor to local memory of the second processor (e.g., fig. 1, el. 800) (Office Action dated 1/19/00, page 10, line 15 - page 16, line 5). Applicants respectfully traverse.

The Aoyama reference discloses a device in which the vector processor comprises a vector register 502 coupling vector arithmetic 501 to address translation 503. Address translation 503 is coupled to main storage 700 (which is external to vector processor (VP)). Accordingly, since main storage 700 is not part of vector processor (VP), it is not an "on-board" local memory or program memory that is part of vector process (VP). The Examiner relies upon col. 8, lines 4 et seq. to support her argument that Aoyama's vector processor contains both a **program memory and a local memory**. The Examiner is obviously relying upon main storage (MS) 1 as being one of the program memory or local memory - e.g., the teaching that "an address generated by the vector instruction address generate circuit 200 is sent to the main storage 1, and a vector instruction read from the main storage 1 is sent to a register 201" (col. 8, lines 12-15). Unfortunately, the Examiner's reliance on Aoyama is misplaced. Aoyama discloses that "the address generate circuit 200 is configured in the same fashion as the scalar instruction read circuit of FIG. 4 (col. 8, lines 9-12). Aoyama further discloses that MS 1 corresponds to main storage 700 in FIG. 1 (col. 5, lines 31-32). Main storage 700 is NOT part of vector processor 500 or scalar processor 600. Accordingly, Aoyama fails to teach or suggest, "a second processor for performing vector processing, said second processor comprising a core, **a program memory and a local memory**", as is required by Claim 6. Moreover, vector processor (VP) has no equivalent to buffer storage 602 of scalar processor 600, which the Examiner relies upon as one of the memories for scalar processor 600.

There is no teaching or suggestion in the art that would have motivated one of ordinary skill in the art at the time of the invention to re-engineer the Aoyama device to include an internal memory, as is required by Claims 36-39, without the improper hindsight provided by Applicants' disclosure. As a result, Claim 36-39 stand allowable.

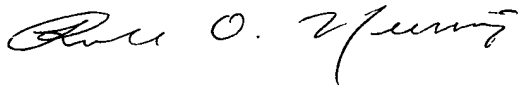
Further, Aoyama discloses two common memories - common memory 800a and main storage (MS) 1 or 700. If the Examiner decides that both , then it further fails to teach or suggest,

"**one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor**", as is required by Claims 36, 37 and 39.

An amendment after a final rejection should be entered when it will place the case either in condition for allowance or in better form for appeal. 37 C.F.R. 1.116; MPEP 714.12. This amendment places the case in condition for allowance. At a minimum, this amendment should be entered because it reduces the number of issues for appeal.

Claims 6-15, 17, 19 and 34-39 stand allowable over the cited art and the application is in allowable form. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418